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Packaging and Test of Photonic Integrated Circuits (PICs)

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The chief commercial advantage of the PIC is in its reduction in the number of component coupling and packaging steps. The result is greater reliability, lower cost and power, and smaller size.

Ivan P. Kaminow (2008)

1.1 Introduction

Compared to semiconductor electronic integrated circuits (EIC), packaging and testing of photonic integrated circuits (PIC) require specific methods and processes. It is due to the particularity of their optical I/Os and in some cases the thermal sensitivity of integrated photonic functions. These constraints prevented industrial processes to reach the same cost breakdown as electronic ICs: today, the major part (up to 80%) of a photonic module cost still lies in packaging and test operations, not in the circuit itself. As explained previously in this book, various technologies exist to fabricate PICs, using various types of materials and structures, with few standards or roadmap relating to packaging and testing.

PIC integration into a module follows an assembly sequence which includes wafer-level test, chip dicing, coupling of optical I/Os to an optical fiber or a laser diode, electrical interconnect to an EIC, and finally the PIC integration into a package or onto a module board. These main steps will be examined in this chapter, reviewing also the main challenges, guidelines, and technologies required by next-generation photonic modules, such as photonic chiplets or photonic interposers.

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1.2 Challenges and Specificities of PIC Packaging and Test

Integration of PICs into a module, embedded in a system (e.g. a switch unit in a 1U blade used in a datacenter rack) requires several specific steps, which will contribute to the final module cost. The final packaged device has to meet the application specifications in terms of operating temperature and environmental standards (e.g. Telcordia GR-468-CORE: Generic Requirements for Optoelectronic Devices Used in Telecommunications Equipment). Figure 1.1 shows a typical assembly flow, involving a silicon photonics-based circuit to achieve a high data rate (e.g. 400 Gbps) datacom transceiver module for intra data center interconnects.

This typical assembly flow is shared by most of PIC-based modules, with slight variations depending on the targeted application and performances. For example, for data rates of 25 Gbps per channel and above, photoreceivers may require high bandwidth transimpedance amplifiers (TIA) add-ons, flip-chipped onto Photonic chips [1] using copper pillar interconnects to lower parasitics and shorten wire length. Figure 1.2 shows the motherboard of a previously released 40 Gbps datacom silicon photonics-based transceiver from Luxtera (10 Gbps per channel).

As well as for semiconductor devices, PICs packaging and testing are mainly driven by interconnects management. Interconnects achieve the PIC connection to the motherboard, sometimes through an intermediate printed circuit board or package (e.g. BGA laminate, or ceramic package). Quite obviously, by contrast to EICs, two types of PICs interconnects can be distinguished:

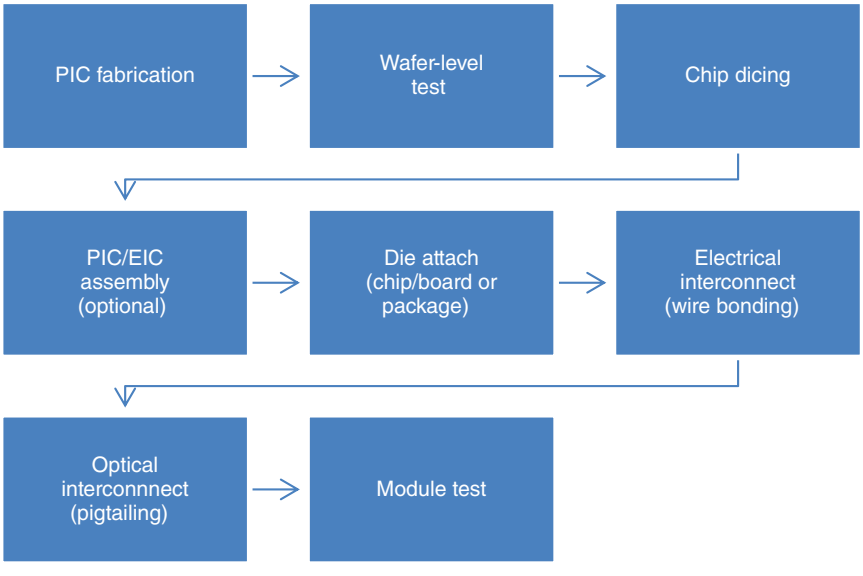

Figure 1.1 Typical assembly flow for the packaging of a silicon photonics PIC into a datacom transceiver module.

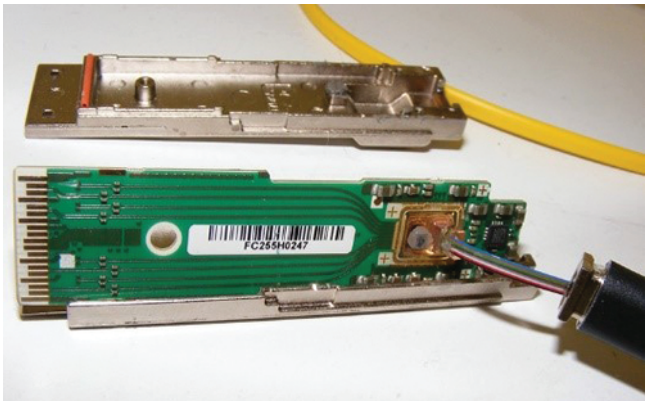

Figure 1.2 Typical content of a silicon photonics module (with QSFP chassis). Source: C. Kopp, CEA-Leti.

- **Optical interconnects**, allowing the connectivity of the PICs integrated optical waveguides to an external waveguide, for example, an optical fiber, with a maximized transmitted optical power. Optical coupling may be the most discussed obstacle to achieve low-cost photonics. By contrast to laser diode packaging, optical coupling of PICs generally involves multiple optical channels, leading to the use of fiber ribbons or multicore fibers (MCF). Fibers are thus mounted into glass V-groove fiber arrays (FA) to be handled during test or packaging processes.
- **Electrical interconnects**, which may be an RF line allowing the proper transmission of a high data rate modulated electrical signal to or from an integrated active photonic device (e.g. phase modulator, photodiode).

1.2.1 Optical Interconnects

From the earliest demonstration of planar waveguide circuits, the challenge of low loss, high yield connection to an optical fiber, or another external waveguide (e.g. a III–V laser) has been identified as a key challenge to allow further adoption of the PIC technology at an industrial level. These challenges are fairly independent on the PIC fabrication technology (lithium niobate oxide, doped glass, silicon photonics, polymer), especially when single-mode waveguides are considered [2–4]. In this chapter, we will focus on single-mode waveguides, which can be found in many application fields, especially in the long-range telecommunications, data center high-speed interconnects, and may compete with VCSEL links for short reach interconnects such as CPU to memory in the near future.

The main parameter that has to be optimized for efficient optical interface – actually, by targeting the lowest possible value – is the coupling loss (CL). It is related to the linear coupling efficiency η, which is the ratio between the coupled optical power into the external waveguide (P_1) and the available optical power at the output of the PIC optical port (P_0), by Eq. (1.1)

$$\mathrm{CL\ (dB)} = -10 \log \eta = -10\ \log \frac{P_1}{P_0} \tag{1.1}$$

This CL is a positive value and it is typically wavelength dependent. Some authors use the logarithmic coupling efficiency $CE = 10\log(\eta)$, which is negative. Additional to the CL, some applications require the amount of reflected power to the input waveguide to be minimized. This results in reducing the corresponding return loss (RL), defined as $RL = -10\log(P_r/P_0)$, where P_r denotes the reflected optical power.

Analytical expression of the CL can be obtained by using Kolgelnik's electromagnetic theory of laser beams. In the case of single-mode waveguides, the coupling efficiency is obtained by calculating the overlap integral between the respective field amplitudes of the fundamental modes E_0 and E_1 related to the PIC and the external waveguide (secondary waveguide) (Eq. (1.2)), in a reference plane (x, y) orthogonal to the z optical axis

$$\eta = \frac{\left|\iint E_0(x,y)\cdot E_1^*(x,y)\,\mathrm{d}x\,\mathrm{d}y\right|^2}{\iint |E_0(x,y)|^2\mathrm{d}x\,\mathrm{d}y\cdot\iint |E_1(x,y)|^2\mathrm{d}x\,\mathrm{d}y} \tag{1.2}$$

References [5–9] provide expressions of η, in the case the output beam from the PIC can be approximated by a Gaussian beam with a waist denoted ω. This approximation is valid for most of the optical waveguide obtained by microtechnologies fabrication processes.

Several cases can be distinguished here. The simplest coupling scenario that could be considered is **butt coupling**, with no gap between the two waveguides. In this case, E_0 is the amplitude of the field at the output of the PIC, and E_1 is the amplitude of the external waveguide's field. Another possible configuration is the case of **lens-assisted coupling**: one or several lenses are inserted between the PIC and the external waveguide, allowing beam refocusing of the PIC's beam to the external waveguide input plane. The same Eq. (1.2) should be used, considering E_0 as the field obtained by propagating the PIC's output beam through the optical system, overlapping with the external waveguide at the entrance plane of the latter.

In the case of a perfect alignment of the waveguide's axis, Eq. (1.2) can be solved analytically, considering the respective beam's waists radii ω_0 and ω_1 (Eq. (1.3)), in the axes x and y, respectively.

$$\eta = \frac{4}{\left(\frac{\omega_{0x}}{\omega_{1x}} + \frac{\omega_{1x}}{\omega_{0x}}\right)\left(\frac{\omega_{0y}}{\omega_{1y}} + \frac{\omega_{1y}}{\omega_{0y}}\right)} \tag{1.3}$$

From this equation, the **mode-matching condition** can be determined: the maximum coupling (i.e. minimum CL) is obtained for $\omega_{0x} = \omega_{1x}$ and $\omega_{1y} = \omega_{1y}$. Whether the considered external waveguide is a laser diode, an optical fiber, or another PIC, an optimum packaging or probe test of a given PIC will target a minimum CL by achieving this condition.

In addition, an analytical expression of η can also be obtained in the case of optical axis misalignment (caused by an offset or a tilt): this leads to the knowledge of the **alignment tolerances** of the system, which is a key parameter to be considered at the packaging or the test level. A convenient way to evaluate alignment tolerance is to calculate the misalignment (tilt or offset) resulting in a 1 dB excess CL (called

"1 dB tolerance"). For lateral misalignment of circular beams (perpendicularly to the optical z-axis) the 1 dB tolerance is given by Eq. (1.4) [10], with waists expressed in micrometers.

$$\eta_{(1\text{ dB})} = 0.33\sqrt{\left(\omega_0^2 + \omega_1^2\right)} \tag{1.4}$$

Depending on the PIC fabrication technology and the nature of the optical waveguide, it may be not possible to reach the mode-matching condition. Knowing the waist parameters will however enable to calculate optimum coupling and alignment tolerances by solving the analytical equations or by simulating coupling by using dedicated software (beam propagation modeling or physical optical propagation module from optical design softwares).

1.2.2 Coupling Structures

Coupling structures are PIC features enabling the light extraction/injection from/into the PIC, possibly including some spot size converter (SSC) function to achieve the mode-matching condition when connection to an optical fiber or another external waveguide is needed. Indeed, in many cases, the used integrated waveguide exhibit mode waists much smaller compared to the waist of the external waveguide due to the use of high index material for the photonic waveguide (e.g. Si or InP) – in the case of silicon photonics, it can be submicrometric. The most critical configuration is for pigtailing (coupling to a single-mode optical fiber) as the fiber's waist (aka mode field radius or MFR) of a standard single-mode fiber (SMF) is typically about 5 μm in the telecommunication wavelength range.

One can distinguish between three types of coupling structures [11–13]. Depending on the used configuration, mode-matching condition (and thus minimum CL), operating wavelength range, polarization-dependent loss (PDL), misalignment tolerance, and manufacturing scalability may be different.

1.2.2.1 Edge Coupler

This kind of structure enables lateral (in plane) direct coupling to an optical fiber or a laser diode by locally modifying the beam waist of the guided mode at the proximity of the PIC facet, if required. It is a broad wavelength solution, with low PDL (<1 dB). Several edge couplers are reported in literature, depending on the waveguide technology. Waveguides with large cross sections (approx. 10×10 μm) exhibit large waists and can be directly coupled to a SMF by dicing and polishing the chip facet. For SiN, InP, or thick SOI waveguides, simple edge coupling without any spot size conversion leads to the use of lensed fiber to achieve the mode-matching condition (waists are typically in the 1–3 μm range). For silicon photonics relying on thin SOI (typically 220 nm thick), SSC is required to achieve waists compatible with commercialy available lensed or flat cleaved fibers.

Spot size conversion is obtained by:

- gradually increasing the physical size of the waveguide (**3D adiabatic taper**) along light propagation axis (z-axis).

- using **inverted tapers**, gradually reducing the lateral waveguide size in the *z*-axis, down to the minimum possible size at the tip (defined by the used lithographic node), resulting in a decrease of the effective index and thus a less confined mode.
- use of **metamaterial structures** exhibiting low effective index.
- adiabatically transferring of the optical power to a **super waveguide** made of another material of lower index (e.g. silicon nitride on the top of a tapered silicon waveguide).

All these different structures (Figure 1.3) provide beam enlargement, with alignment tolerances directly related to the beam size; however, a suitable surface quality of the facet requires polishing at the die level (after dicing or cleaving) or a final etching process step performed at the wafer level. In any case, wafer-level test remains challenging.

1.2.2.2 Vertical Grating Coupler (VGC)

Vertical grating coupler (VGC) relies on diffractive elements integrated at the end of a PIC waveguide (Figure 1.4), deflecting the propagating beam out of plane, at nearly 90° (current designs target 82°), while intrinsically converting the beam size. This feature is very popular in silicon photonics-based circuits, as the high

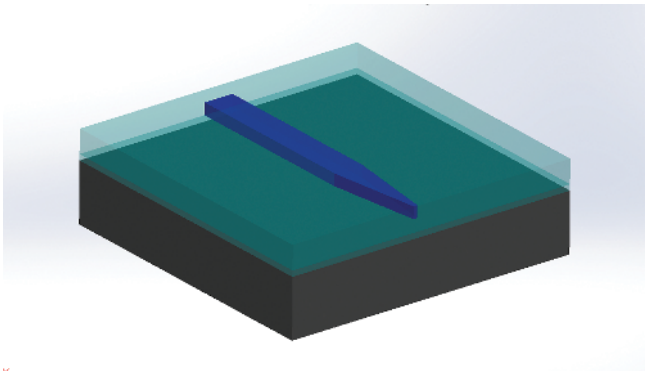

Figure 1.3 Edge coupling structure obtained by inverted taper design. Source : S. Bernabé, CEA-Leti.

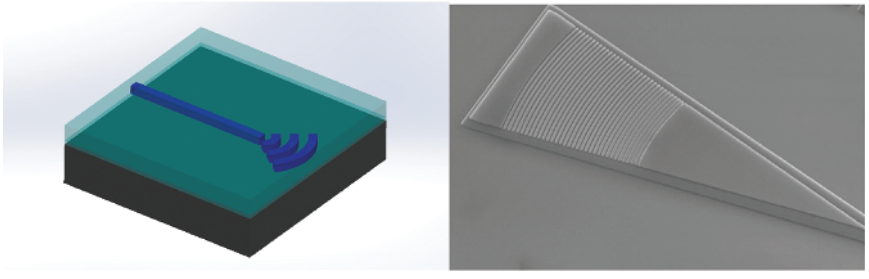

Figure 1.4 Scheme and SEM view of a single polarization grating coupler (SPGC). Source: S. Bernabé, CEA-Leti.

index contrast of silicon waveguide core to silica cladding allows high diffraction efficiency of periodical or quasi-periodical gratings. VGC enables mode matching with SMF, making wafer-level test and multifiber packaging much more convenient compared to edge couplers. Additionally, VGCs can be placed at any location on the PIC surface, and do not require any post-process such as polishing or cleaving. VGC exhibits limited bandwidth (<30 nm) and polarization dependency which can be improved to <0.5 dB by designing two-dimensional structures, sometimes referred to as 2D-VGC. These structures, close to photonic crystals arrays, act as polarization splitters/combiners, with typical CL of 3.5 dB [12].

Arrays of VGC can also be used to enable coupling to a multi core fiber (MCF).

1.2.2.3 Evanescent Coupling

This approach, which allows efficient wavelength-dependent coupling between two adiabatically tapered waveguides (Figure 1.5), has been basically used to perform rough testing of earlier generations of waveguide. It relies on the evanescent coupling in a region where the two deconfined modes overlap.

Through optimization of tapered designs, it is now possible to use it to achieve efficient coupling from a buried waveguide in the PIC to an external waveguide positioned above it, at an optimum distance. This external waveguide can be embedded in a flex substrate, or be a polished or tapered fiber. This configuration typically exhibits large (>50 nm) 1 dB tolerance along the waveguide optical axis (z-axis), and is intrinsically broadband in terms of spectral bandwidth [11].

1.2.3 Wafer-level Test

In the past years, wafer-level test strategies have been developed to test PICs with similar processes as for semiconductor chips. Particularly, wafer-level test aims at enabling a deep range of measurements and tests at the end of the chip fabrication process, allowing a screening of the fabricated chips and identification of known good dies (KGD) before the packaging steps. Here also, the specificity of PICs in terms of optical I/Os prevents from directly applying test techniques developed for microelectronics circuits – i.e. probe tester-based wafer-level test. These well-known test methods need to be slightly adapted, depending on the type of used coupling structures and the complexity of electro-optical (E/O) tests to be performed.

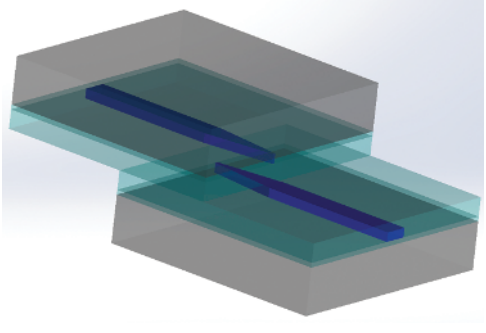

Figure 1.5 Evanescent coupling between two PICs with adiabatic couplers. Source: S. Bernabé, CEA-Leti.