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Introduction

1.1 Different Interfaces in OFETs

When Nobel laureate Herbert Kroemer coined the famous phrase that “the interface is the device” [1], he pointed out the essential importance of the interfaces between different materials in any device action, especially for semiconducting thin-film devices, which have shown astonishing successes in photonic and electronic applications. From the point of view of a typical organic field-effect transistor (OFET), the device performance is mainly determined by the properties of the materials used and their corresponding interfaces. In general, an OFET [2–5] consists of three electrodes (source, drain, and gate), a dielectric layer, and an organic semiconductor (OSC) layer (Figure 1.1). To improve the device performance and even build novel functionalities, interface engineering of these heterojunctions is currently a research focus because of its promising potential for further applications in broad areas ranging from integrated circuits and energy conversion to catalysis and chemical/biological sensors [6–14]. In fact, scientists in a variety of disciplines have been devoting great efforts to this concept, which started with simple improvement of the device performance and has branched out in different directions, indicating the interdisciplinary of these efforts [15–18]. In comparison with traditional complementary metal oxide semiconductor transistors, the advantages of OFETs originate from how they can be manufactured, including considerable variety in molecular design, low cost, light weight, mechanical flexibility, solution processability, and large-area fabrication.

There are four major contact interfaces in OFETs, namely, the interface within the semiconductor layers, semiconductor/electrode interface, semiconductor/dielectric interface, and semiconductor/environment interface (Figure 1.2). In general, the interface within the semiconductor layers [19, 20] contains traps, grain boundaries, and other defects, which provide scattering sites for carriers and are detrimental to charge transport (Figure 1.2a). Recent studies [21, 22], however, proved that semiconductor doping and blends had a positive influence on the crystallinity and morphology of the semiconductor films. Several strategies have been developed to achieve high-quality thin films, as well as to form good heterojunctions, thus affording ambipolar OFETs that are useful for building future OFET-based integrated

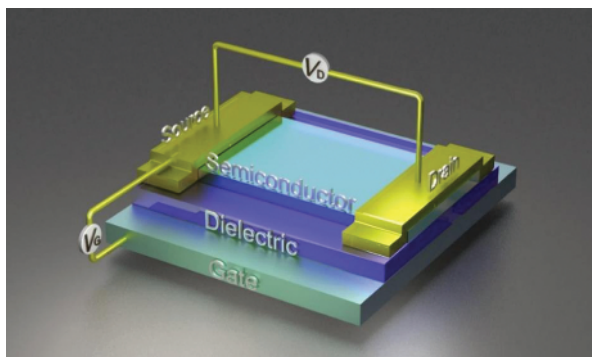


Figure 1.1 Schematic illustration of a typical OFET architecture.

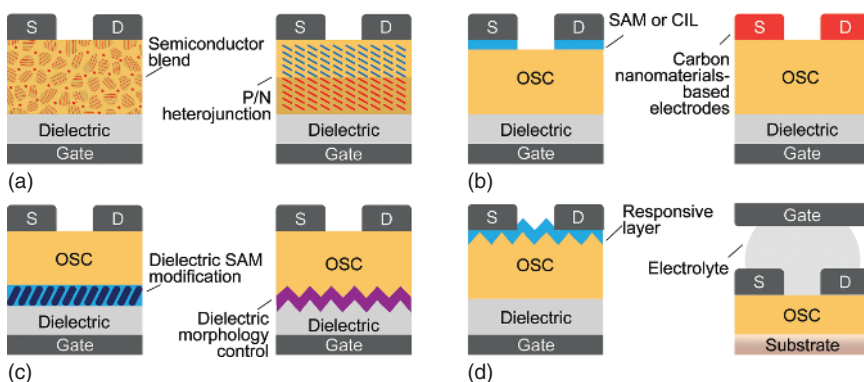


Figure 1.2 Interface engineering of interfaces in OFETs. (a) Interface within the semiconductor layers, (b) semiconductor/electrode interface, (c) semiconductor/dielectric interface, and (d) semiconductor/environment interface. SAM: self-assembled monolayer; OSC: organic semiconductor; CIL: charge insertion layer.

devices, accelerating charge separation, and improving the device performance. By designing mixed or segregated crystal heterojunctions made of OSCs, functional devices such as photodetectors, memory devices, and ambipolar transistors can be realized.

Another important interface in OFETs is the semiconductor/electrode interface (Figure 1.2b) [9, 23–25], which usually determines the efficiency of charge-carrier injection and extraction. By carefully choosing the self-assembled monolayer (SAM) or charge insertion layer (CIL) to modify metal electrodes, the charge-injection barrier can be fine-tuned at the interface, which could significantly reduce the contact resistance between semiconductors and electrodes, thus enhancing the device performance. More interestingly, by using functional layers, whose molecular conformation or electronic structure can be switched by external stimuli, the properties of OFETs can respond to external signals. This concept sets the foundation for building functional devices such as optical/electrical switches, memories, and photodetectors.

The semiconductor/dielectric interface is a vital interface [26, 27] that dominates carrier transport (Figure 1.2c) because (i) charge carriers are generated at the interface and (ii) the electrical current path is through at most the first few layers of molecules at the interface. In addition, the surface energy and microstructure of the dielectric interface have a significant impact on the local morphology of the semiconductor layer. Therefore, modification of this interface by SAMs or stimuli-responsive layers offers an important and universal methodology to improve the device performance and to even integrate new molecular functionalities such as photo-controllable memories, superconductors, and charge-trap memories into organic electrical circuits.

The semiconductor/environment interface is useful for building functional OFETs for sensing applications [12, 13, 15, 17, 28–30] (Figure 1.2d) by directly exposing the semiconductor layer to the environment being analyzed. This method offers some valuable advantages over other technologies, such as label-free capability, real-time detection, and compatibility with both the biological system and the electronics industry. Some intrinsic drawbacks, however, hamper the use of OFET-based sensors for practical sensing applications. The first is the diffusion of the analyte into grain boundaries in the semiconductors, causing either trapping or doping of charge carriers. This could result in serious problems such as device instability and irreversibility because of the physically destructive interaction between semiconductors and analytes. Second, because of the signal amplification characteristics of OFETs, any nonspecific response or noise would cause interference with the intrinsic signal of the analytes, leading to a pseudo-signal and poor selectivity. Therefore, rational control of interfacial charge transport is crucial to control the doping effects, increase the sensing selectivity/sensitivity, and even install new functionalities.

1.2 Brief Historic Overview of Interface Engineering in OFETs

We have summarized in Figure 1.3 the key developments to give a comprehensive big picture of the interface-engineered functional OFETs. Starting from the first demonstration [31, 32] of OFETs in the 1980s to their very recent applications [21, 29, 30] in skin electronics, the performance and functionality of OFETs have evolved simultaneously and promoted each other, shedding light on their potential applications in healthcare, wearable electronics, and degradable electronics.

1.3 Scope of the Book

In this comprehensive *book*, we aim to provide a systematic survey of recent significant advances in developing effective methodologies of interface engineering in OFETs, from fundamental models to experimental techniques, for creating high-performance and multifunctional optoelectronic devices. In Chapter 2, we

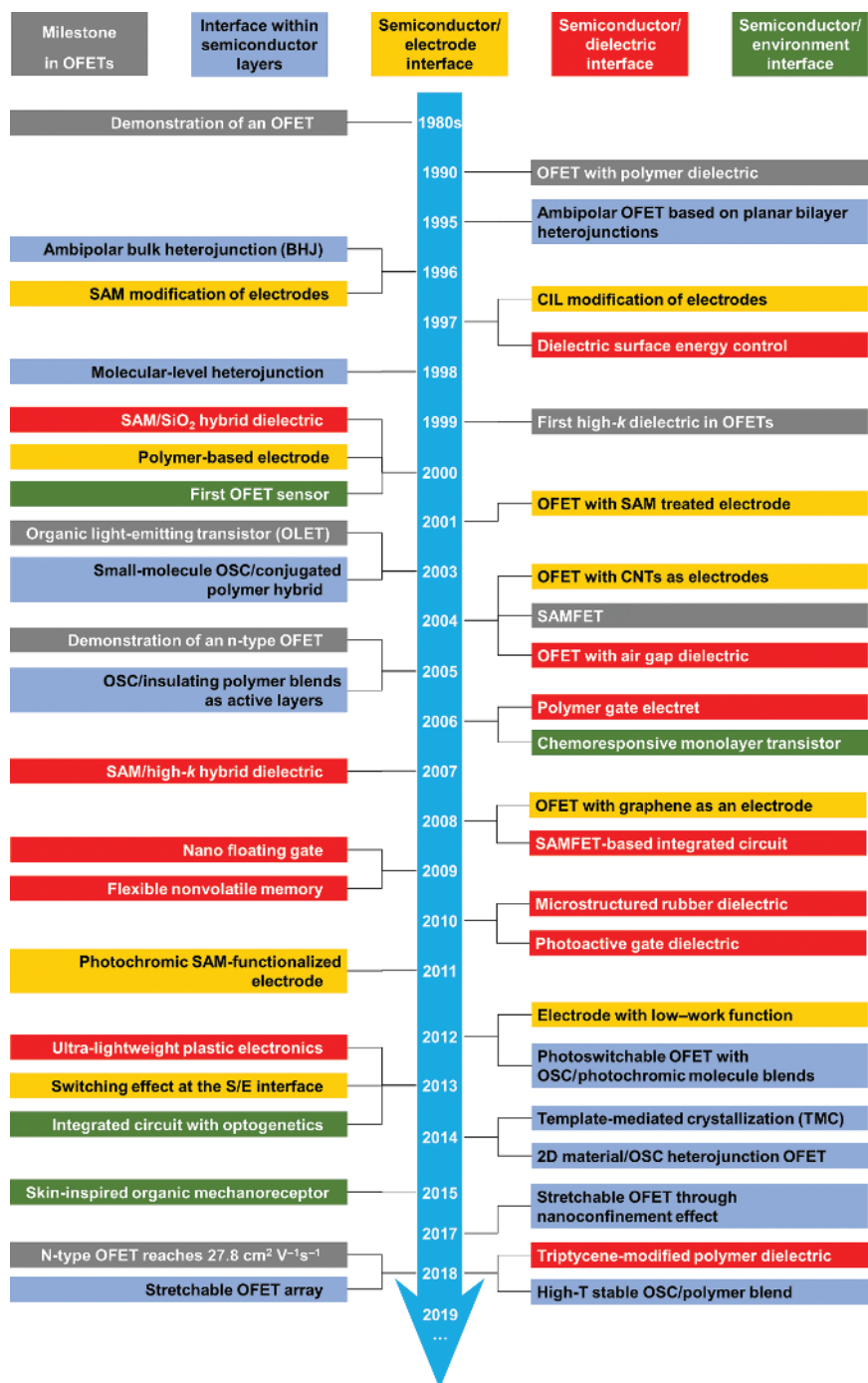


Figure 1.3 Timeline showing key developments in interface-engineered functional OFETs [10, 21, 25, 28, 29, 31, 32, 37, 57, 71, 74, 77, 81, 114, 137, 143–145, 160, 168, 172, 180, 187, 205, 237–240, 298, 312, 315, 326, 331, 333, 348, 353, 359–361, 376, 393, 397, 417, 447, 459].

will summarize interfacial modification methods in OFETs, which include physical and chemical modification methods. We will not go into details of them. Instead, summative tables and figures will be present to compare each method. Then, we focus on how to use interface engineering strategies to improve the inherent properties of OFETs at the semiconductor/semiconductor interface (Chapter 3), semiconductor/electrode interface (Chapter 4), semiconductor/dielectric interface (Chapter 5), semiconductor/environment interface (Chapter 6), as well as interfacing organic electronics with biology (Chapter 7). Both are of great importance to lie the foundation of the OFET research. We also provide a critical discussion of the limitations and main challenges that still exist for the development of practical applications in Chapter 8. Such a book will be invaluable for better understanding fundamental charge-transport mechanisms at the interfaces and will offer novel insights into the device design concept, the device fabrication process, and the development of future multifunctional practical transistors.

